

Koneru Lakshmaiah Education Foundation

(Category -1, Deemed to be University estd. u/s. 3 of the UGC Act, 1956)

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07-05-2020

Webinar

on

""High-Level Hardware Synthesis Using VIVADO_HLS"

Circular:

4/3/24, 3:14 PM

Mail - HOD-ECE - Outlook

ECE Webinar (6) on "High Level Hardware Synthesis Using VIVADO_HLS" on 06-05-2020 & 07-05-2020-Reg.

HOD-Department of Electronics and Communication Engineering <hod.ece@kluniversity.in> Tue 05-05-2020 11:20

To:ECE Faculty <ecefaculty@kluniversity.in>;eceteaching@klh.edu.in <eceteaching@klh.edu.in>;KLH Director <director@klh.edu.in>;koteswararao@klh.edu.in <koteswararao@klh.edu.in>;ALL HODS <hods@kluniversity.in>;All Deans <deans@kluniversity.in>;Suman Maloji <suman.maloji@kluniversity.in>;ECSEFACULTY14 <ECSEFACULTY14@kluniversity.in> Cc:PRINCIPAL - COE <principal.coe@kluniversity.in>;Vice Chancellor - KLU <vc@kluniversity.in>;PRESIDENT <president@kluniversity.in>

1 attachments (217 KB) Webinar 6, ECE.jpg;

Respected Sir/Madam,

In the series of webinars, the sixth webinar is scheduled and the details are as follows.

Webinar: "High Level Hardware Synthesis Using VIVADO_HLS"

Speaker: Mr. P. Srikanth Reddy, Asst. Professor , ECE Dept.

Expert Talk Series: 06

Date: 06-05-2020 & 07-05-2020

Time: 10 AM

Register Here:



https://forms.gle/TAnpcJetERNpq9zK6

Interested faculty are requested to register using the above mentioned link. All HODs are requested to share the details in the respective department.

Thank You,

Dr. Suman Maloji M.Tech., Ph.D Professor and Head Department of Electronics and Communication Engineering (DST-FIST Snonsored Department) Koneru Lakshmaiah Education Foundation (Deemed to be University estd., u/s 3 of UGC Act 1956) Green Fields, Vaddeswaram 522502. Guntur Dt., Andhra Pradesh, INDIA.

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Poster:



Fig. Poster of webinar

1. Objective and discussions:

High-Level Hardware Synthesis (HLS) using Vivado HLS is a process of converting highlevel language descriptions (such as C, C++, or SystemC) into RTL (Register Transfer Level) hardware descriptions for FPGA (Field-Programmable Gate Array) implementation. Vivado HLS is a tool provided by Xilinx for this purpose. Here's an introduction to high-level hardware synthesis using Vivado HLS:

- 1. **Design Entry**: The process begins with writing or generating a high-level description of the hardware functionality using a supported high-level language, such as C, C++, or SystemC. This description represents the algorithm or behavior that you want to implement in hardware.
- 2. **Vivado HLS Tool**: Vivado HLS takes the high-level description as input and automatically generates RTL code (typically VHDL or Verilog) that implements the same functionality. The tool performs various optimizations and transformations to ensure the resulting RTL code meets timing constraints and resource utilization targets.



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- 3. **Directive-Based Optimization**: Vivado HLS allows users to guide the synthesis process through directives (also known as pragmas) embedded in the high-level code. Directives provide hints to the tool on how to optimize the hardware implementation. For example, directives can specify loop unrolling, pipeline initiation interval (II), resource allocation, and interface customization.
- 4. **Verification**: After synthesis, the generated RTL code needs to be verified to ensure it behaves as expected. Vivado HLS provides simulation capabilities for verifying the functional correctness of the synthesized hardware. You can use testbenches and stimulus to simulate the RTL code and compare the results with the original high-level description.
- 5. **Integration with Vivado Design Suite**: Once the RTL code is verified, it can be integrated into a larger FPGA design using the Vivado Design Suite. Vivado HLS generates IP (Intellectual Property) cores that can be instantiated in Vivado projects alongside other IP cores and custom logic.
- 6. **Performance Analysis**: Vivado HLS provides performance estimates during synthesis, allowing designers to analyze metrics such as clock frequency, throughput, and resource utilization. This helps in optimizing the design further for better performance and area efficiency.
- 7. **Iterative Design Process**: High-level hardware synthesis using Vivado HLS enables an iterative design process where designers can quickly explore different algorithms and optimizations at a high level of abstraction before committing to a specific hardware implementation.

In summary, Vivado HLS offers a productive workflow for converting high-level language descriptions into efficient hardware implementations for FPGA-based systems, allowing designers to leverage their software expertise to accelerate FPGA development.

Online Link

https://us02web.zoom.us/j/?pwd=dngeertndgkseeRGDETcdiafkf49

Number of participants: 88



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Close	
DK	Dr. K. Praghash 🖊 🂆 >
	Dr. Mvd Prasad 🗾 🗾 🖉 🎽 >
DN	Dr. Naren Das 🗾 🗾 🗾 🗾 🗾
DP	Dr. P. Pardhasaradhi 🛛 🗾 🏂 >
DP	Dr. Preetham reddy C S 🛛 🗾 🏂 >
DR	Dr. Rakesh Palisetty 🛛 📈 🎉 >
DK	Dr.Aswin Kumer S V 🛛 🗖 🏂 >
D	Dr.S.Sunithamani 🗾 🗾 🖉 >
DR	Dr.Srinivasa Rao K. 🗾 🗾 🖉 >
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Chat	ts Invite Mute All Unmute All

Fig. List of participants

List of the Participated Students: 38

S. No.	Roll No	Name
1	180040255	SHAIK TAPA SABEENA
2	180040266	DASETTY LAVANYA



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